Williams-Kilburn CRT early computer memory

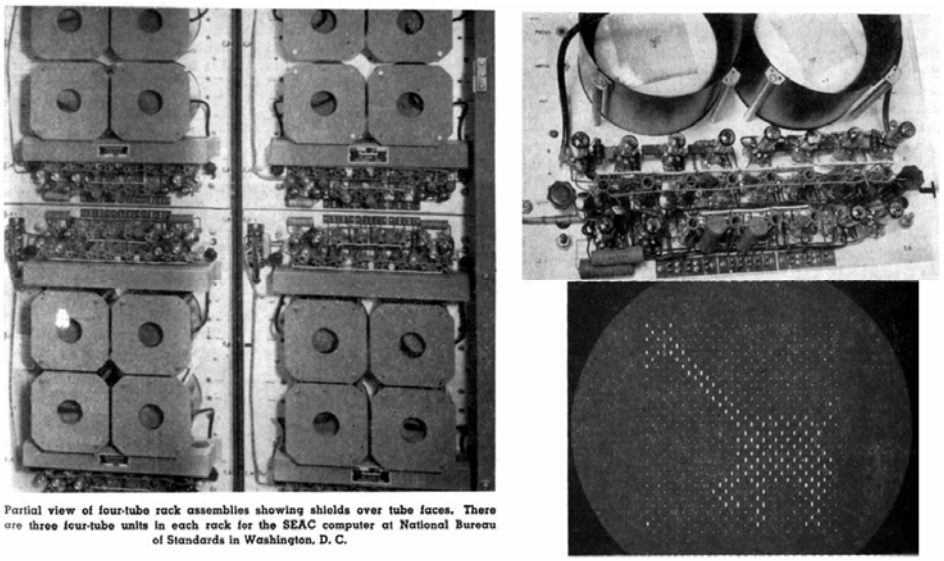
After the war Frederic Williams and Tom Kilburn at University of Manchester developed a digital memory using a cathode-ray tube, CRT, to store binary data in form of dots or dashes on the screen. This memory exploited the phenomenon of charge persistence for a short while in the area of the screen hit by electrons. This kind of CRT memory was a pseudo-random-access one. Either this type or the sequential access type based upon a delay-line were used in early digital computers up to the introduction of ferrite core memories in 1954.

The charge storage effect was not dependent upon a specific CRT, provided it granted the proper spot resolution. Several 3-inch or 5-inch tubes were used for the purpose, with data capacity of 1024 or 2048 bits per tube.

- The CRT memory developed by NBS

In December 1953, Electronics described the CRT computer memory array developed by US National Bureau of Standards. Even if Williams and Kilburn explained the operation of their system basing upon the well-known theory of secondary-emitting surfaces, there were some not well-explained phenomena. Nevertheless, CRT memories, based upon the Williams storage system, were used for their high speed. In US, to take full advantage of their speed, memory banks were often built with a word-wide parallelism. In this case, a battery of 45 cathode ray tubes was used to store words each 45 bit wide. Read or write speeds of 21,000 words per second were obtained. By the way, similar speeds were obtained with some quartz delay line memory units.

Several cathode ray tubes were satisfactory tried in the described array, 5UP1, 5UP11 and also 3KP1. Here are some pictures of the memory, showing a group of CRTs and details of a pair of tubes with shields removed; in these pictures also video amplifiers are visible. The third picture shows the pattern of stored bits on a repeater monitor.



Partial view of four-tube rack assemblies showing shields over tube faces. There are three four-tube units in each rack for the SEAC computer at National Bureau of Standards in Washington, D. C.

Fig. 1 - Left, internal view of a CRT memory rack, showing groups of two CRTs, each with its associated Read/Write/Refresh circuitry. Right, a closeup view of two storage tubes with front shields removed and image of the memory content, as seen on the screen of an auxiliary monitor oscilloscope.

A dot-dash mode of operation was chosen, dashes being written in the ‘one’ locations. The X and Y deflection plates of the 45 tubes were connected in parallel, driven by a staticizer counter with two

power DACs. 4 bits were used for the X-axis and 5 bits for Y, resulting in a total capacity of 512 words. Each DAC used three 807s in the output stage, to drive an equivalent load of 1200pF through a 100V swing, with 3µs settling time. A sequencer generated a 0.5µs write/read pulse to drive the grids of the CRTs, plus a 0.25µs read strobe pulse and a ramp superimposed on the Y deflection signal. If a 'one' was detected on the read strobe, the write pulse was stretched to 2.5µs. A block diagram of the memory system is given in fig. 2. The simplified schematics of the gating amplifier, which has a gain as high as 30.000, and of the X deflection circuit are given in fig. 3.

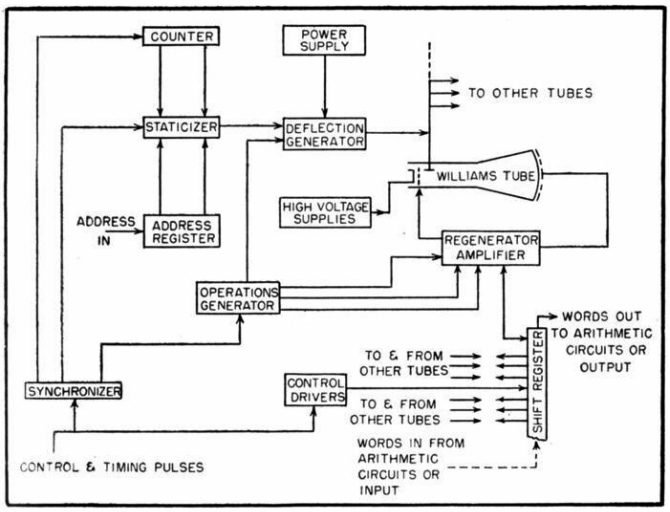


FIG. 5—Block diagram of electrostatic memory system using modified conventional cathode-ray tube

Fig. 2 - Block diagram of the memory system.

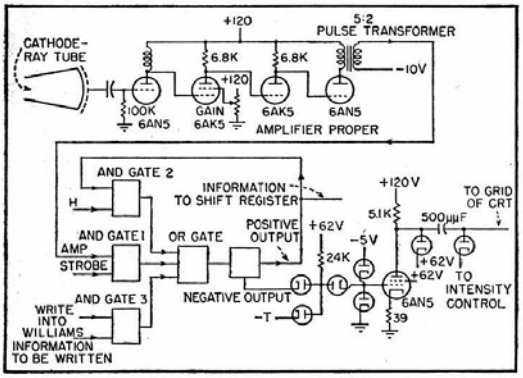


FIG. 7—Gating-amplifier circuit employed in Williams system for Bureau of Standards SEAC computer

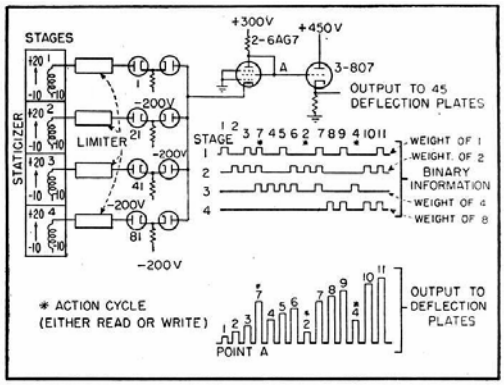


FIG. 8—Binary address digits are converted to weighted currents and summed before being applied to plates

Fig. 3 - Simplified schematic diagrams of the sense amplifier, left, and of the X-deflection circuit, right.

Stored data need to be continuously regenerated. This function is performed sequentially for each of the memory positions and is intermixed with the computer read/write access. Every location access takes 12µs, regardless of whether it is a read/write or a refresh cycle. Therefore a new refresh of the entire array takes place every 6144 microseconds, or every 6 milliseconds.