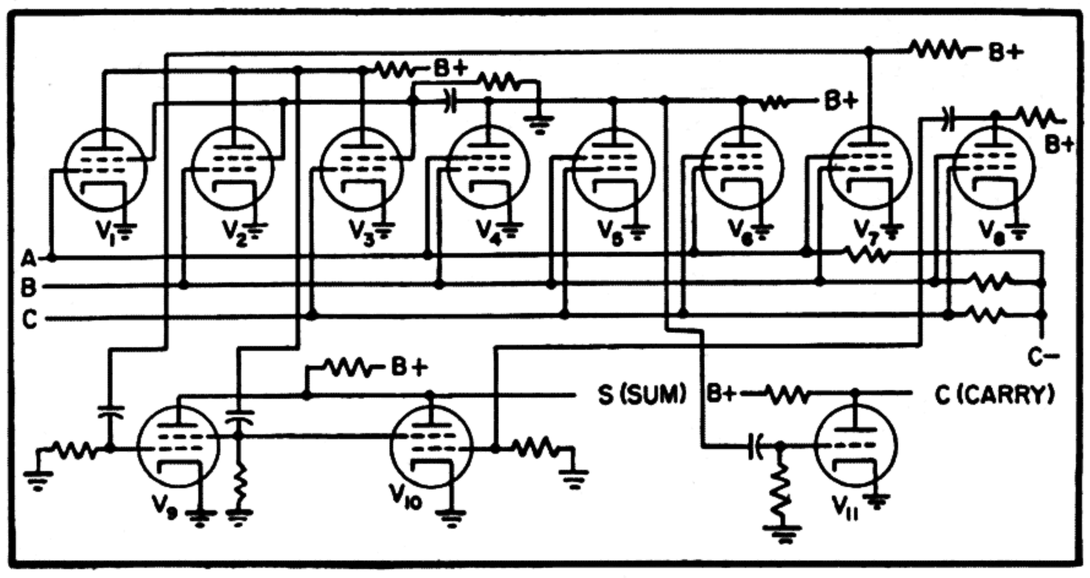

FIG. 1—Typical binary adder developed from pentode tubes

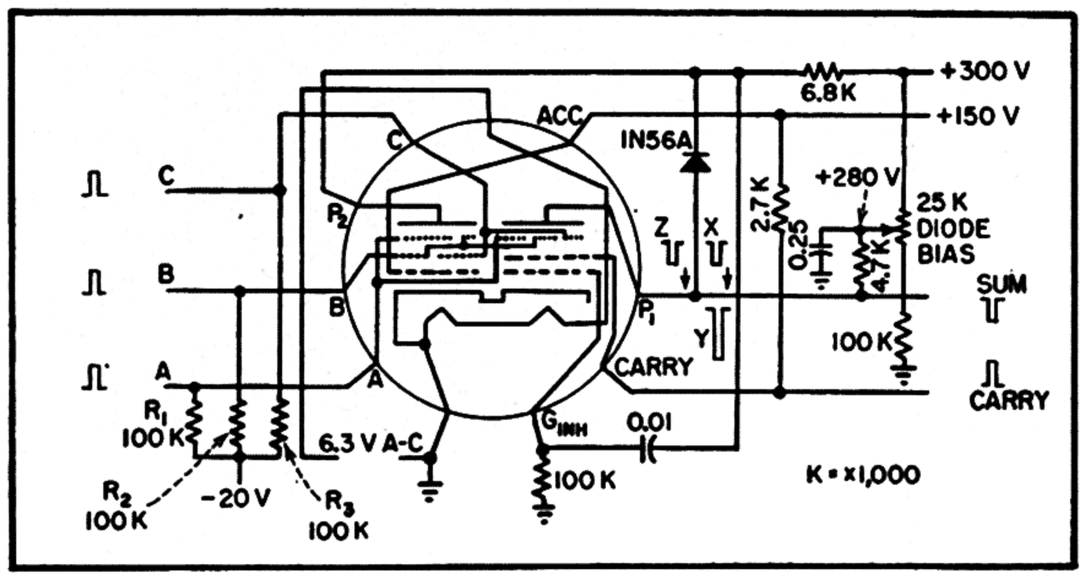

FIG. 2—Binary-adder tube replaces array of Fig. 1

Binary Adder Tube for High-Speed Computers

SUMMARY —— Special-purpose electron tube has all required binary-addition functions self-contained in single envelope. Outputs have sufficient power to insure sharp rise times with fast operational speeds and will directly drive similar following tube without additional amplification

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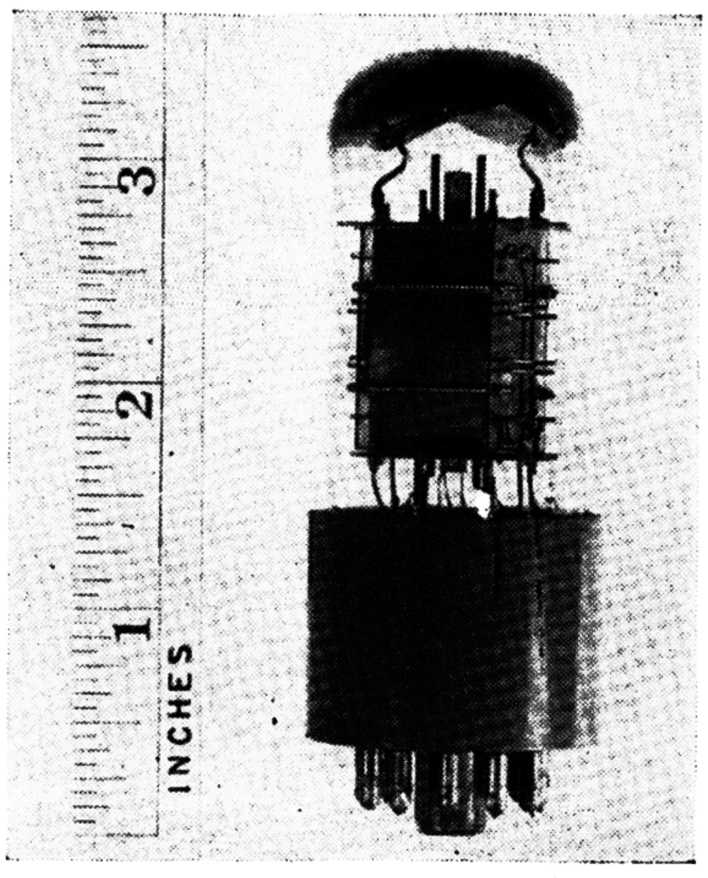
THREE-INPUT binary adders are conventionally developed by combining a number of simple elements or gates which have the required functions: and; or; inhibitor. This generally results in a complicated circuit of tubes, diodes or relays.

A typical adder developed from pentode electron tubes is shown in Fig. 1. This makes an excellent adder. However, the complete array must be repeated for each digital place to be added causing the number of components to become large, especially in the case of a several-place parallel binary adder.

All of the functions of the array of Fig. 1 may be accomplished in the single BG2 binary-adder tube illustrated in the photograph.



Experimental tube is sealed in T-9 bulb with 11-pin neosubmagnal base

A schematic of the tube structure and associated circuit is given in Fig. 2.

The mount structure consists of a central flat cathode surrounded by two half sections of grids and plates.

Three grid inputs, *A*, *B* and *C*, are internally connected to control grids in both halves of the tube. These grids are externally biased to cutoff through grid resistors R_1, R_2 and R_3.

Two outputs are provided. Plate P_1 produces a negative sum pulse

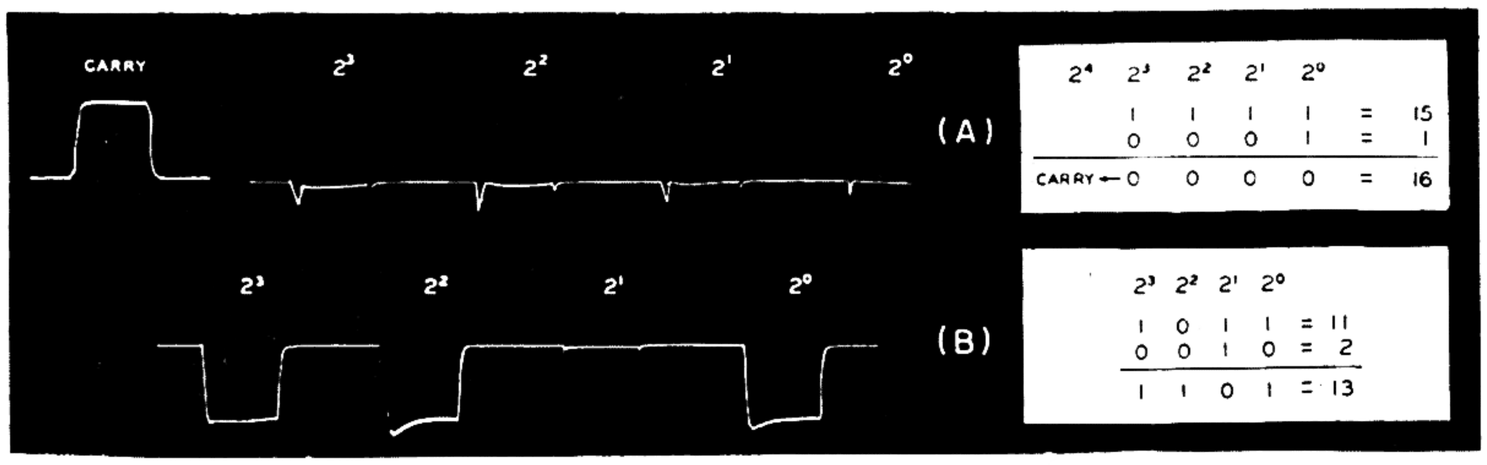


FIG. 3—Inhibited sum pulses and through carry in sample addition (A); sum pulses in sample addition (B)

in the event A, B or C is opened by a positive signal. The carry output produces a positive signal identical to the input signals, in the event any two or all three of the inputs are opened. During a double coincidence, however, no sum signal is produced. On a triple coincidence, both sum and carry signals are produced.

Operation

In the left half of the tube, as shown in Fig. 2, there is an accelerator grid which plays no part in the dynamic action. Following this is a set of three compound control grids so arranged that no electrons are gated to P_2 unless there is a double or triple coincidence of inputs on grids A, B and C. The output signal developed on P_2 is different in these two cases. On any double coincidence, one third of the grid area is opened, which produces a 20-volt negative signal on plate P_2.

On a triple coincidence, the entire grid area is opened, producing an approximately 60-volt negative signal on P_2.

Either of these two signals is sufficient to cut off completely inhibitor grid G_{inh} in the right half of the tube. These signals are shown on the feedback loop from P_2 to G_{inh} as waveforms X and Y and enter G_{inh} through the blocking capacitor. These signals are also offered a path from P_2 to P_1 across the 1N56A diode. However, the positive end of this diode is biased 20 volts negative with respect to the no-signal voltage on P_2. The small signal X from P_2 cannot cause any potential change on the P_1 or sum output since it does not exceed the bias. The large 60-volt signal Y is able to override this bias resulting in a negative difference signal Z on the sum output.

Grid G_{inh} is biased to cathode potential and is therefore normally conducting. Following this grid is an accelerator element which is connected to a high positive voltage through a 2,700-ohm load resistor. This is the carry element. It draws current in the normal condition and hence is negative with respect to B+. Following the carry element are three signal grids, internally connected to the ABC inputs, which are normally cutoff.

Electrons which drift through the carry element are gated to P_1 if any of these grids are opened. Thus any single coincidence on A, B or C will produce a sum signal on P_1. A double or triple coincidence will also tend to produce a signal on P_1 except that the negative signal produced on P_2 inhibits the electron flow by cutting off G_{inh} as has been previously described. Thus no sum signal is produced on P_1 at any other time than on a single coincidence.

Since a sum signal is required on a triple coincidence input and this is prevented from forming directly on P_1 because of the inhibiting, it is derived as the signal Z across the diode as described. When G_{inh} is driven negative on either a double or triple coincidence the carry element ceases to draw current and goes strongly positive. This produces an amplified positive carry pulse capable of directly driving another adder tube input.

Characteristics

Since this tube is a digital device operating only in the regions of cutoff and saturation, the important qualities are clean cutoff and high electron perveance. Since there is no requirement that this be a small-signal device, a reasonable input pulse amplitude of 20 volts positive was selected as an operating goal and all signal grids were adjusted to give cutoff values of −12 to −15 volts. The inhibitor grid has a somewhat sharper cutoff at about −10 volts which contributes materially to the rise time of the carry pulse. This section has an available gain factor of about 30.

The carry element acts not only as an accelerator but as the output element of the most important signal from the tube. This has been designed to dissipate continuously about 2½ w at a current of 15 ma.

Currents to plates P_1 and P_2 are approximately 3 ma. The static accelerator element ACC draws approximately 10 ma or 1.5 watts and is designed to dissipate this power continuously. A 6.3-volt, 0.8-ampere heater is used.

In a cascaded parallel-adder system the accumulation of delay in the carry is inherent and cannot be eliminated. This is so regardless of the components used in the adder. The delay arises from the fact that whereas the inhibitor signal and the sum signal are generated simultaneously by the input signals, the inhibitor signal must take the time to charge another grid before the sum signal can be shut off. This action generates the carry which in turn must charge another grid input in the next stage. Thus there are two delays in series at each stage. If this carry must generate another inhibitor signal and carry in the second stage, it is now delayed by a factor of 4.

Delay Spikes

The delay appears on the sum outputs as a leading-edge spike. Its width at any given output depends on the following factors: (1) the inherent rise time of the inhibitor system; (2) the inherent rise-time of the carry system; (3) the number of previous stages a carry has traversed.

The spike on the first 2^0 stage will always be small, since only the first factor is of consequence. On any succeeding stage it may be the same or some greater width up to (1) + (2) + (3) n, where the nth tube in n stages will be the worst case in certain additions, but in others will

be no worse than the first sum output.

An example of this widening spike during the progress of a carry through several stages is shown in Fig. 3A for a worst case in adding the binary 15 + 1. Note the proportionate narrowing of the carry pulse in the 2^4 place.

Another example of addition is shown in Fig. 3B, in which a carry resulting from the addition of addend and augend pulses in the 2^1 place generates the sum signal in the 2^2 place.

The measured carry delay with the type BG2 tubes and recommended circuit constants is about 0.3 μsec per stage, maximum. This would result in a worst-case spike of approximately 3 μsec in a ten-stage adder.

In the case of serial addition, as shown in Fig. 4A, there is no accumulation of carry delay. The very slight delay due to the first and second factors mentioned above can be partly compensated by slightly overdelaying the carry signal in the feedback path. The sum outputs will have somewhat narrower spikes than even the best case of parallel addition. This should contribute greatly to the ultimate speed.

This tube was designed specifically to operate in a several-stage a-c coupled parallel adder similar to the circuit in Fig. 4B. In this set-up it was found to work at pulse rates up to 100 kc in a four-stage adder. However, if a larger number of stages were used the speed would be reduced to the point where the worst-case spike could be differentiated from the sum pulse.

In a serial addition application, such as shown in Fig. 4A, a considerably faster operational speed can be obtained.

Applications

There are some other logical functions aside from straight binary addition to which this tube may be adapted. One of these is the two-input Boolean adder or anti-coincidence detector. For this application the bridging diode and carry resistor are not needed and the third input grid is biased permanently to C−. The sum plate, P_1, will give the same outputs on $A = 0$ and $B = 0$ as on $A = 1$ and $B = 1$. Only the anticoincidence of A or B gives an output. Simultaneously if desired, the carry output could be used to separate the positive (11) coincidences and the negative (00) coincidences.

Another function may be added with a fourth input on G_{1mh}. By biasing this grid to cutoff by removing the feedback loop from P_2 and applying a positive signal D, sum outputs occur on coincidences of any ABC inputs with D, but not on any ABC coincidences without D, and not, also with D alone.

The tube could also be used as an ABC coincidence detector by feeding the P_2 signal to G_{1mh} through a biased diode. This bias should be such that the small double-coincidence signal from P_2 will not cut off G_{1mh} but the much more negative triple-coincidence signal will. The carry output would then give a signal only on an ABC coincidence. This signal will be in phase with the input signals.

Some interesting flip-flop and oscillator circuits can be designed around this tube. Since the carry output is in phase with the signal input, this may be fed back to one of the inputs with either d-c coupling to give flip-flop action or a-c coupling to give oscillation.

The following is an example of a different logical function which can be done in this way. Suppose some event could only be made to occur by the arrival of two elements A and B. Once started, however, the presence of either A or B would maintain the event and only the absence of both would cause it to cease.

This can be done with the BG2 tube by feeding back the carry into an input, say the C input. Direct-current coupling is assumed on both this feedback and the P_2-G_{1mh} feedback loop. Since the carry element is normally negative, grid C will remain closed. To form an inhibitor signal on P_2 it is necessary to open two inputs. Therefore, in this condition, nothing except a sum output will happen on either A or B inputs. However, if A and B are both activated, the carry is formed, which now opens input C. Thus if either A or B drops out, there are still two grids open and the flip condition will maintain. However, if both A and B drop out, the system will reset to the original condition and maintain that way until another A-B coincidence.

This development has been sponsored by an agency of the Department of Defense.

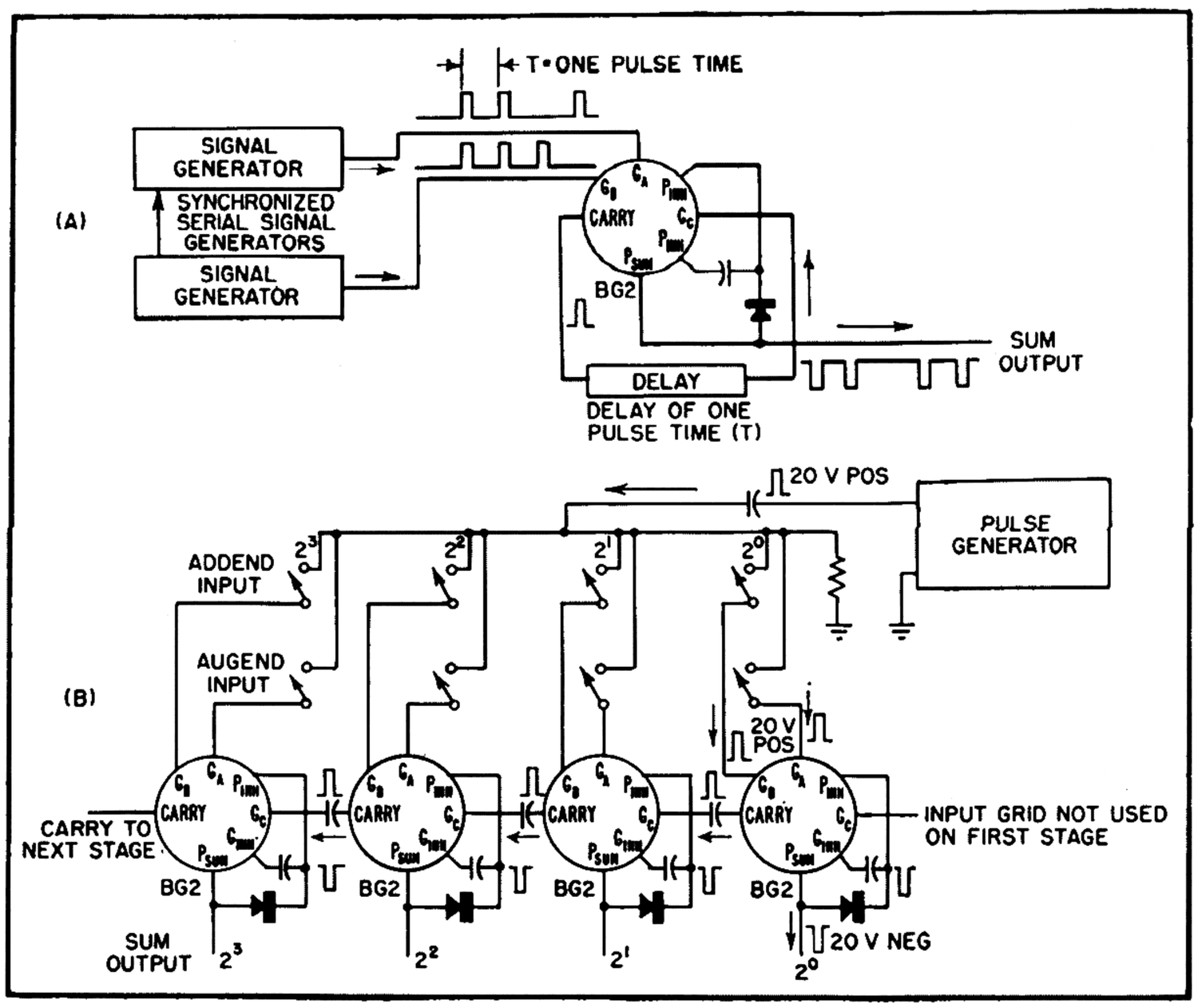


FIG. 4—Demonstration serial adder (A) and parallel adder (B), use BG2 binary-adder tubes. Serial adder can have operational speed in the region of 1 mc